GaN-TYPE ENHANCEMENT MOSFET USING HETERO STRUCTURE

Inventor(s): Fan Ren
Cammy R. Abernathy
Stephen J. Pearton
Yoshihiro Irokawa

UNIVERSITY OF FLORIDA

(UF Disclosure No. 10861)

AKERMAN SENTERFITT DOCKET No.: 5853-274

GaN-TYPE ENHANCEMENT MOSFET USING HETERO STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application 60/405,964 entitled "GaN-TYPE ENHANCEMENT MOSFET USING HETERO STRUCTURE" filed on August 26, 2002, the entirety of which is incorporated herein by reference.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002] The United States Government has rights in this invention pursuant to Grant No. N00014 99 1 0204 between the Office of Naval Research and the University of Florida.

Field of the Invention

[0003] The invention relates to an enhancement mode metal oxide semiconductor field effect transistor (MOSFET) formed from a Group-III nitride compound semiconductor.

Background

[0004] Historically, device performance improvements have been achieved by scaling. However, fundamental limits to device scaling are being reached and problems related to scaling are becoming more significant. Currently, Si-based power devices are generally used in high power electronic devices. However, their performance has almost reached the value predicted by theory and can no longer be significantly improved. Accordingly, alternative devices based on different substrates capable of providing improved performance have been under investigation.

[0005] One area that still has not been fully exploited is the engineering of substrates to achieve higher carrier mobility. Gallium nitride (GaN), which is a Group-III nitride compound semiconductor, has a large forbidden band gap, equal to about 3.4 eV. The indirect transition conduction band is positioned at a level higher than the forbidden band by more than 1.5 eV. The saturation velocity of GaN is approximately 2.5. x 10^7 cm/s, which is higher than other types of semiconductors, such as silicon (Si), gallium arsenide (GaAs), and silicon carbide (SiC). Further, the breakdown electric field of GaN is approximately 5 x 10^6 V/cm, which is greater than SiC, and greater than Si and GaAs by more than one order of magnitude. Thus, GaN has physical characteristics that are suitable for use in high-frequency, high-temperature, and high-power semiconductor devices.

[0006] A conventional FET using GaN is a Schottkey gate transistor having a metal semiconductor (MES) structure. An n-type GaN active layer is formed on a sapphire substrate with an intrinsic-GaN buffer layer therebetween. A gate electrode, a source electrode, and a drain electrode are disposed on the active layer.

[0007] An alternate Schottkey gate FET structure, referred to as a high electron mobility transistor (HEMT) structure, includes an electron transit layer made from impurity-undoped GaN and an electron supply layer made from n-type AlGaN which are sequentially laminated on a substrate, such as a sapphire substrate. A gate electrode is formed on the electron supply layer, and a source electrode and a drain electrode are disposed on the electron transit layer on both sides of the electron supply layer.

[0008] In another example of known GaN based FETs having the HEMT structure, the thickness of the AlGaN electron supply layer is decreased, thereby making the threshold gate

voltage around 0 V. This type of FET is referred to as a "enhancement-mode FET", but is not a true enhancement mode FET as it does not require a positive gate voltage to turn on.

[0009] In the foregoing MES or HEMT-structured FETs, the Schottky barrier at the gate electrode between a metal and the semiconductor is comparatively low, such as approximately from 1 to 1.2 eV. Although this Schottky barrier is slightly greater than that of the GaAs-type FETs (0.7 eV), a large forward gate bias voltage cannot be applied. This shortcoming originates from the operation of the MES-structured FET rather than from the constituent material, such as GaN.

[00010] In contrast, large forward gate bias voltages are possible from a conventional metal-oxide-semiconductor field effect transistor (MOSFET), where the substrate generally used is silicon. In this type of FET, a gate electrode is formed on a Si layer with a silicon oxide (SiO_2) film therebetween. The silicon dioxide film provides a highly electrically insulating film. For enhancement-type MOSFETs, an inversion layer is formed at the Si interface between the SiO_2 film and the Si layer through application of a sufficient gate to body (or source) voltage.

[00011] N-channel GaN based depletion MOSFETs of MOSHEMTs have been realized without the need for impurity doping in the channel region. AlGaN/GaN heterojunctions experience large piezoelectric effects which generate a large interface charge. The large interface charge can induce an electron sheet in the GaN near its interface with AlGaN.

[00012] Some have disclosed GaN based depletion mode MOSFETs. Some have even claimed to disclose "enhancement mode GaN based MOSFETs". However, the disclosed "enhancement mode GaN based MOSFET" devices are not truly enhancement mode devices since an enhancement MOSFET is characterized as a MOS device which forms a channel only

when the gate to body (or source) voltage exceeds some threshold voltage. Accordingly, there is a need for true GaN based enhancement mode MOSFETs.

SUMMARY OF THE INVENTION

[00013] A GaN-based enhancement mode MOSFET includes a GaN comprising layer and a (Group III)x$Ga_{1-x}N$ layer, where x is from 0 to 1, such as Alx$Ga_{1-x}N$, disposed on the GaN comprising layer. Although the Group III element will be referred to herein as being Al, the group III element can be other Group III species, such as B, or mixtures thereof.

[00014] The thickness of the Alx$Ga_{1-x}N$ layer is less than 20 nm. This provides negligible sheet carrier concentration in the GaN layer at its interface with $Al_xGa_{1-x}N$ to permit enhancement mode operation. Typically, at some $Al_xGa_{1-x}N$ thickness value from 10 to about 20 nm, the device will become a depletion mode device for any thickness above this value.

[00015] A source and a drain region extend through the $Al_xGa_{1-x}N$ layer into the GaN layer, the source and drain region separated by a channel region. A gate dielectric is disposed over the channel region. The gate dielectric layer can be SiN_x, MgO or Sc_2O_3. A gate electrode is disposed on the gate dielectric. The MOSFET formed is a true enhancement MOSFET which is in an off-state when the gate is unbiased.

[00016] The parameter x is preferably from 0.2 to 0.35. The enhancement MOSFET can be either an n-channel or a p-channel device.

[00017] The $Al_xGa_{1-x}N$ layer can be undoped or p-doped. The thickness of the $Al_xGa_{1-x}N$ layer can be less than 10 nm, less than 5 nm, or more preferably from 1 to 4 nm thick.

[00018] The GaN comprising layer can be p-GaN, undoped GaN or InGaN. In one embodiment of the invention, a p-AlGaN or undoped AlGaN layer can be disposed below the GaN comprising layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[00019] A fuller understanding of the present invention and the features and benefits thereof will be accomplished upon review of the following detailed description together with the accompanying drawings, in which:

[00020] FIG. 1(a) illustrates an n-channel GaN based enhancement mode MOSFET according to an embodiment of the invention.

[00021] FIG. 1(b) illustrates an n-channel GaN based enhancement mode MOSFET according to an alternate embodiment of the invention.

[00022] FIG. 2(a) illustrates the band-structure for the p-AlGaN/GaN heterojunctions for the AlGaN/GaN MOSFET transistors shown in FIGs. 1(a) and 1(b) with no applied voltage to the gate.

[00023] FIG. 2(b) illustrates the band-structure for the p-AlGaN/GaN heterojunctions for the AlGaN/GaN MOSFET transistors shown in FIGs. 1(a) and 1(b) evidencing two inversion channels.

DETAILED DESCRIPTION OF THE INVENTION

[00024] A GaN-based enhancement mode MOSFET includes a GaN comprising layer and a (Group III)$_x$Ga$_{1-x}$N layer disposed on the GaN layer, where x is between 0 and 1. As noted earlier, although the Group III element will be referred to herein as being Al, the group III element can be other Group III species, such as B, or mixtures thereof.

[00025] The thickness of the $Al_xGa_{1-x}N$ layer to provide enhancement mode operation is below a certain thickness. By providing a $Al_xGa_{1-x}N$ layer thickness of approximately 20 nm or less, such as 10 nm, preferably less than 5 nm, and more preferably from 1-4 nm, negligible sheet carrier concentration in the GaN layer at its interface with $Al_xGa_{1-x}N$ results. Accordingly, the surface of the GaN adjacent to the $Al_xGa_{1-x}N$ layer can be rendered undoped or even p-type. A source and a drain region each extend through the $Al_xGa_{1-x}N$ layer into the GaN layer, the source and drain region separated by a channel region.

[00026] A gate dielectric is disposed over the channel region. A gate electrode is disposed on the gate dielectric. The MOSFET formed is a true enhancement MOSFET which is in an off state when the gate is unbiased.

[00027] Regarding the composition of the $Al_xGa_{1-x}N$ layer, x can be from .05 to 1.0. Preferably, x ranges from 0.2 to 0.35.

[00028] The invention can be used to produce a true enhancement mode GaN based MOSFET. Thus, the invention provides at least two significant advantages as compared to conventional MOSFETs. First, the thin AlGaN surface layer can protect the GaN channel from being damaged during the deposition of the gate oxide layer. This leads to higher carrier mobility in the GaN layer. Second, the transistor structure forms a GaN quantum well at AlGaN/GaN

interface, which can provide better carrier confinement, improved carrier mobility and carrier concentration.

[00029] The invention can be embodied as either a p-channel or n-channel MOSFET. In the case of an n-channel MOSFET, an epitaxial layer stack comprising p-type or undoped AlGaN and GaN can be used. To form a p-channel MOSFET, an epitaxial layer stack comprising n-type or undoped AlGaN and GaN can be used. Thus, using undoped base epi, both n-channel MOSFETs and p-channel MOSFETs can formed using the same epitaxial layer stack. When non-complementary structures are not required for a given application, the invention is preferably embodied using n-channel MOSFETs due to their improved performance as compared to p-channel MOSFETs.

[00030] Two exemplary embodiments of n-channel enhancement MOSFETs according to the invention are shown in FIGs. 1(a) and 1(b), respectively. Referring to FIG. 1(a), transistor 100 includes gate electrode 110 disposed on gate dielectric layer 115. Gate dielectric layer 115 can be any suitable dielectric, such as SiO_2, SiNx, MgO or Sc_2O_3. Gate dielectric layer 115 is disposed on a thin layer of p-type or undoped AlGaN 120. It may be possible to replace the Al in layer 120 with certain group III elements, such as boron.

[00031] The thin AlGaN layer 120 is disposed on a p-type or undoped GaN layer 125 to form a vertical heterostructure. Although not described in detail herein, the invention can also be used to form vertical MOSFETs. In a vertical MOSFET, the gate and source contacts are on the front of the substrate the drain is located on the back side of the substrate. The advantage of vertical MOSFETs is that the breakdown voltage from drain to source can be extremely high since the drift region for the vertical MOSFET is the entire thickness of the substrate.

[00032] Transistor 100 also comprises n+ source 130 and n+ drain 135 regions. The depth of regions 130 and 135 is preferably 300 to 400 nm. For example, Si or Ge can be used as the n dopant. The thickness of the AlGaN layer 120 can be from about 0.5 nm to about 20 nm, preferably being about 4 to 5 nm.

[00033] However, if a p-AlGaN layer 120 thicker than about 10 nm is used, the device performance will generally be degraded as compared to a thinner p-AlGaN layer 120 due to longer distance between the gate 110 and the inversion channel (not shown). If the p-AlGaN layer 120 comprises a thick undoped AlGaN layer, such as > 20 nm, an n-channel will generally be formed at the AlGaN/GaN interface due to the piezoelectric effect. This will result in the formation of a depletion mode n-channel MOSFET device.

[00034] To form a p-channel enhancement mode MOSFETs, the steps described above for forming an n-channel MOSFET can generally be repeated, except an undoped or n-type AlGaN and GaN layer stack is provided, rather than p- or undoped AlGaN and GaN. For example, n-type GaN can comprise Si-doped GaN. P+ source and drain regions, such as magnesium doped regions, are then formed in the AlGaN/GaN layer stack, such as through ion implantation of Mg or selective area re-growth of Mg-doped GaN.

[00035] Transistor 100 provides a heterojunction layer between AlGaN layer 120 and GaN layer 125. Since AlN has a band gap of about 6.4 eV which is almost double as compared to GaN (about 3.3 eV), AlGaN can be appropriately treated as an insulator as compared to the GaN layer. Therefore, transistor 100 can form both a first inversion layer at the surface of AlGaN layer 120 adjacent to gate dielectric layer 115, as well as a second inversion layer in the GaN layer 125 near the AlGaN/GaN interface. Since GaN has lower energy band gap, the inversion channel in the GaN layer 125 at the AlGaN/GaN interface will be at a lower threshold voltage as

compared to the first inversion layer formed at the surface of AlGaN layer 120 adjacent to gate dielectric layer 115.

[00036] An alternate embodiment of an n-channel enhancement mode transistor 150 is shown in FIG. 1(b). Transistor 150 includes gate electrode 160, disposed on gate dielectric layer 165, which is disposed on a thin layer of p-type or un-doped AlGaN 170. The AlGaN layer is disposed on a layer of InGaN 175, which is disposed on a layer of AlGaN 180. Thus, transistor 150 includes two vertical heterostructures.

[00037] Transistor 150 includes n+ source 185 and drain 190 regions. The depth of regions 185 and 190 is preferably from about 300 to 400 nm.

[00038] Figure 2(a) shows the band-structure for the p-AlGaN/GaN heterojunctions for the AlGaN/GaN MOSFET transistors shown in FIGs. 1(a) and 1(b) with no applied voltage to the gate. In this state, no n-channel exists in both the AlGaN 120 and GaN layer 125 since the conduction band edge (E_c) is above the Fermi level (E_f) for both layers. Thus, assuming the device does not punchthrough from source to drain, negligible current will flow between the source and drain even if a large voltage is imposed between the source and the drain. Thus, the device formed is clearly a true enhancement mode device.

[00039] As the gate to source voltage of n-channel enhancement mode transistor 100 or 150 is increased to some positive ("threshold") voltage above the source or body voltage, an inversion channel 250 between the AlGaN layer 120 and the GaN layer 125 will generally be first induced. As the gate voltage is further increased, a second inversion channel 240 at the interface between the gate dielectric 115 and the AlGaN layer 120 is generally also induced, thus providing two inversion n-channels. Figure 2(b) shows the band structure following application of a sufficiently positive voltage to the gate relative to the source or body of the device to create

n-channels 240 and 250. As a result of the band structure shown in FIG. 2(b), electrons can easily flow between the source and drain upon application of a voltage between the source and drain. With the gate voltage removed, no channel is present and the device is in an off state. Thus, devices according to the invention can provide a normally-off, enhancement mode power MOSFET.

[00040] The invention can find applications in inverter systems, analogous to a standard Si based CMOS inverter layouts for use in high power electronics. Significantly, the invention can generally be operated at high temperature without a cooling system, because GaN is a wide band gap semiconductor and the switching loss of the enhancement mode FETs according to the invention is low. Enhancement mode devices use less power as compared to depletion mode devices because enhancement mode devices, unlike depletion mode devices, generally consume little or no power during stand-by mode. Thus, the invention can reduce switching loss.

[00041] The invention may also provide improved breakdown voltages as compared to other available structures. A voltage across a gate of a MOSFET produces an electrical field which is distributed through the oxide and semiconductor, the magnitude of which is proportional to the dielectric constant of the oxide. The dielectric constant of MgO and Sc_2O_3 which can be used for the gate oxide 115, are much higher than that of SiO_2. Accordingly, the gate to source or body breakdown voltage of the GaN MOSFET should be higher as compared to a GaN MESFET or a Si-MOSFET. Also, the use of high dielectric constant oxide layers permit use of thinner oxide layers. This arrangement provides higher drain current and transconductance.

[00042] An ideal market for the invention is for high power electronics devices. For example, for automobile applications where circuits must withstand a high temperature environment

without additional cooling systems, such as beyond the capabilities of Si-based technology (e.g. > 200 °C) or more, the invention can be particularly useful.

[00043] It is to be understood that while the invention has been described in conjunction with the preferred specific embodiments thereof, that the foregoing description as well as the examples which follow are intended to illustrate and not limit the scope of the invention. Other aspects, advantages and modifications within the scope of the invention will be apparent to those skilled in the art to which the invention pertains.